IN THE CLAIMS:

The pending claims are as follows:

1. (Previously and currently Amended) A Dynamic Random Access Memory (DRAM), comprising:

a plurality of strip-type active areas on a substrate;

a plurality of strip-type shallow trench isolation regions on the substrate for isolating each of the active areas, the active areas and the shallow trench isolations being alternatively and parallel arranged on the substrate;

a plurality of word lines above the active areas and the shallow trench isolation regions, an array being formed by overlapping the word lines and the active areas, the array including a plurality of first overlapping portions and a plurality of second overlapping portions, wherein every two of the first overlapping portions are separated by every two of the second overlapping portions on each strip of the active areas and each of the first overlapping portions is next to each of the second overlapping portions on every two neighboring active areas; and

a capacitor array in the active areas, each of the capacitors being in each of the first overlapping portions, the capacitor including a deep trench structure and a collar isolation, a first collar portion being on an adjacent portion of two of the neighboring capacitors, a second collar portion being on a non-adjacent portion of two of the neighboring capacitors, the first collar portion being longer than the second collar portion in a depth direction of the deep trench and a depth of the second collar portion being the same as a depth of the top plate, wherein a memory cell is formed by the word line in one of the second overlapping portions and the capacitor in one of the first overlapping portions.

2. (Original) The DRAM as recited in claim 1, wherein the deep trench structure of the capacitor comprises:

a bottom plate on an interface region of the substrate and a lower sidewall portion of the deep trench structure;

a dielectric layer, formed on an internal surface of the bottom plate; and

a top plate, formed by filling the deep trench structure and covering the dielectric layer with a conductive material.

3. (Original) The DRAM as recited in claim 2, wherein the bottom plate is formed by thermal diffusion with an impurity gas to dope the lower sidewall portion of the deep trench structure.

4. (Original) The DRAM as recited in claim 2, wherein the dielectric layer is a composite layer comprising silicon nitride and silicon oxide.

5. (Original) The DRAM as recited in claim 2, wherein the top plate comprises a polysilicon layer doped with arsenic.

6. (Previously Cancelled)

7. (Currently amended) The DRAM as recited in claim [[6]] 1, wherein a thickness of the first collar portion and the second collar portion is about 400Å-500Å for respectively isolating the neighboring capacitors and sufficiently decreasing a leakage current of the substrate theresurrounding.

8. (Currently amended) The DRAM as recited in claim [[6]] 1, wherein the capacitor further comprises:

a buried strap conductive layer, above the second collar portion, including a diffusion conductive region in the substrate outside the buried strap conductive layer; and

a trench top isolation, above the buried strap conductive layer, wherein the trench top isolation connects with the shallow trench isolation regions in a word line direction.

9. (Original) The DRAM as recited in claim 8, wherein the buried strap conductive layer further comprises a doped silicon layer and the diffusion conductive region is formed by a thermal process on the doped silicon layer.

10. (Original) The DRAM as recited in claim 8, wherein the trench top isolation further comprises a silicon oxide layer.

11. (Original) The DRAM as recited in claim 1, wherein the shallow trench isolation regions further comprises a silicon oxide layer.

12. (Original) The DRAM as recited in claim 1, further comprising a gate oxide layer between the substrate and the word lines.

13. (Original) The DRAM as recited in claim 1, wherein the word line further comprises a doped silicon layer and a silicon tungsten layer as a gate electrode.

14. (Original) The DRAM as recited in claim 8, wherein two sides of each of the second overlapping portion further comprise a source and a drain of each of the memory cell.

15. (Currently amended) A Dynamic Random Access Memory (DRAM), comprising:

a plurality of strip-type active areas on a substrate;

a plurality of shallow trench isolation regions on the substrate for isolating each of the active areas;

a plurality of word lines above the active areas and the shallow trench isolation regions, an array being formed by overlapping the word lines and the active areas, the array including a plurality of first overlapping portions and a plurality of second overlapping portions, wherein every two of the first overlapping portions is separated by every two of the second overlapping portions on each of the active areas, and each of the first overlapping portions is next to each of the second overlapping portions on every two the neighboring active areas; and

a capacitor array on the active areas, each of the capacitors being on each of the first overlapping portions, the capacitor comprising:

a deep trench structure, comprising an upper sidewall region and a lower sidewall region;

a collar oxide layer, on an upper sidewall portion of the deep trench structure, comprising a first collar portion and a second collar portion, the first collar portion being on an adjacent portion of two of the neighboring capacitors, the second collar portion being on a non-adjacent portion of two of the neighboring capacitors, the first collar portion being longer than the second collar portion in a depth direction of the deep trench structure, the first collar portion being used to isolate the neighboring

capacitors and the second collar portion being used to reduce sufficiently a leakage current of the substrate surrounding thereof;

a buried strap conductive layer, above the second collar portion, including a diffusion conductive region in the substrate outside the buried strap conductive layer; and

a trench top isolation, above the buried strap conductive layer, wherein the trench top isolation connects with the shallow trench isolation regions in the word line direction;

wherein a memory cell formed by the word line in one of the second overlapping portions controls the capacitor via the diffusion conductive region in one of the first overlapping portions.

16. (Original) The DRAM as recited in claim 15, wherein the deep trench structure of the capacitor comprises:

a bottom plate on an interface region of the substrate and the lower sidewall portion of the deep trench structure;

a dielectric layer, formed on an internal surface of the bottom plate; and

a top plate, formed by filling the deep trench structure and covering the dielectric layer with a conductive material.

17. (Original) The DRAM as recited in claim 16, wherein the bottom plate is formed by thermal diffusion with an impurity gas to dope the lower sidewall portion of the deep trench structure.

18. (Original) The DRAM as recited in claim 16, wherein the dielectric layer is a composite layer comprising silicon nitride and silicon oxide.

19. (Original) The DRAM as recited in claim 16, wherein the top plate comprises a polysilicon layer doped with arsenic.

20. (Original) The DRAM as recited in claim 15, wherein a thickness of the first collar portion and the second collar portion is about 400Å-500Å.

21. (Original) The DRAM as recited in claim 15, wherein the buried strap conductive layer further comprises a doped silicon layer and the diffusion conductive region is formed by a thermal process on the doped silicon layer.

22. (Original) The DRAM as recited in claim 15, wherein the trench top isolation further comprises a silicon oxide layer.

23. (Original) The DRAM as recited in claim 15, wherein the shallow trench isolation regions further comprises a silicon oxide layer.

24. (Original) The DRAM as recited in claim 15, further comprising a gate oxide layer between the substrate and the word lines.

25. (Original) The DRAM as recited in claim 15, wherein the word line further comprises a doped silicon layer and a silicon tungsten layer as a gate electrode.

26. (Original) The DRAM as recited in claim 15, wherein two sides of each of the second overlapping portion further comprise a source and a drain of each memory cell.

Claims 27-35 (cancelled)

36. (Previously Added and currently amended) A deep trench capacitor for Dynamic Random Access Memory (DRAM), comprises:

a deep trench structure;

a bottom plate on an interface region of the substrate and a lower sidewall portion of the deep trench structure;

a dielectric layer, formed on an internal surface of the bottom plate;

a top plate, formed by filling the deep trench structure and covering the dielectric layer with a conductive material;

a first collar portion being on an adjacent portion of ~~two of~~ the two neighboring capacitors;

a second collar portion being on a non-adjacent portion of ~~two of~~ the two neighboring capacitors, wherein the first collar portion being longer than the second collar portion in a depth direction of the deep trench; and

a buried strap conductive layer~~, above~~ on the second collar portion.

37. (Previously Added) The deep trench capacitor as recited in claim 36, wherein the bottom plate is formed by thermal diffusion with an impurity gas to dope the lower sidewall portion of the deep trench structure.

38. (Previously Added) The deep trench capacitor as recited in claim 36, wherein the top plate comprises a polysilicon layer doped with arsenic.

39. (Previously Added) The deep trench capacitor as recited in claim 36, wherein a depth of the second collar portion being the same as a depth of the top plate.

40. (Previously Added) The deep trench capacitor as recited in claim 36, wherein a thickness of the first collar portion and the second collar portion is about 400Å-500Å for respectively isolating the neighboring capacitors and sufficiently decreasing a leakage current of the substrate theresurrounding.

41. (Previously Added) The deep trench capacitor as recited in claim 36, wherein the capacitor further comprises:

a trench top isolation, above the buried strap conductive layer, wherein the trench top isolation connects with the shallow trench isolation regions in a word line direction.

42. (Previously Added) The deep trench capacitor as recited in claim 36, wherein the buried strap conductive layer further comprises a doped silicon layer and the diffusion conductive region is formed by a thermal process on the doped silicon layer.

43. (Previously Added) The deep trench capacitor as recited in claim 41, wherein the trench top isolation further comprises a silicon oxide layer.

44. (Previously Added) The deep trench capacitor as recited in claim 41, wherein the shallow trench isolation regions further comprises a silicon oxide layer.

45. (Previously Added) The deep trench capacitor as recited in claim 36, wherein the buried strap conductive layer including a diffusion conductive region in the substrate outside the buried strap conductive layer.